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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,545	01/24/2002	Satoshi Kumaki	57454-334	3322

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EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,545	KUMAKI ET AL.	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

INFORMATION DISCLOSURE STATEMENT

1. The Applicant's submission of the IDS (Japanese Patent No. 5-298894) filed 01/24/02 have been considered. As required by **M.P.E.P. 609 C(2)**, a copy of the PTOL-1449 is attached to the instant office action.
However, The Applicant's submission of the IDS (Other Art - "Misubishi Semiconductor Data book 1997 Memory SRAM) " filed 01/24/02 fails to comply with **37 CFR 1.98(a)(3)(i)** because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. As required by **M.P.E.P. 201.14(c)** acknowledgement is made of applicant's claim for priority based on an application filed June 7, 2001 in Japan.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-4, 6-7, 10-12 are rejected under 35 U.S.C.102 (e) as being anticipated by Al-Shamma et al. PN 6,400,633.

3. As per claims 1, 4:

Al-Shamma teaches a data processor comprising: a random access memory; a processing unit carrying out data processing while accessing said random access

memory; a conversion unit [e.g., number of output bits have to be toggled; col. 3, lines 4-6; fig. 3] converting data so that the number of bits having a predetermined value out of said data is at least a predetermined number for output to said random access memory when said processing unit writes said data into said random access memory; a first retain circuit [106, fig. 2; col. 2, lines 50-55] storing previous data output by said processing unit; and a subtracter [108, fig. 1; col. 2, lines 55-58; col. 4, lines 35-40] taking a difference between the previous data stored in said retain circuit and current data output by said processing unit when said processing unit writes data into said random access memory [col. 2, lines 55-60]; [fig. 1-2; abstract; col. 1, lines 53-60; col. 2, lines 39-65; col. 3, lines 1-50]

4. As per claims 2-3:

Al-Shamma teaches conversion unit [108, fig. 1, fig. 2] includes a detection circuit [314, fig. 3] detecting, when said processing unit writes data into said random access memory, whether the number of bits having a first value out of said data is at least the number of bits having a second value differing from said first value [e.g., majority detector circuit 314 (fig. 3) inside power saving circuit 108 (fig. 1) determines that more than a predetermined number of output bits have to be toggled/flipped, col. 3, lines 1-5; col. 3, lines 43-55] to set a flag [e.g., PS (power saving signal) is asserted/not asserted, col. 3, lines 10-15];

a first inversion circuit [310, fig. 3] inverting said data for output, and a first select circuit [310, 320, fig. 3] responsive to the flag set by said detection circuit to selectively provide said data and said inverted data output from said first inversion circuit to said random access memory [fig. 3-4; col. 3, lines 20-40];

a second inversion circuit inverting data output from said random access memory for output, and a second select circuit [318, 306, fig. 3] responsive to flag to selectively provide data output from random access memory and inverted data output from second inversion circuit to processing circuit when processing circuit reads out data from random access memory col. 3, lines 10-60].

5. As per claims 6-7:

Al-Shamma teaches a first detection circuit [314, fig. 3] detecting a data write timing of a predetermined period including the write timing of the first data out of the data write timing into said random access memory by said processing unit; and a first selector [310, fig. 3] selecting data output from said processing unit at the timing detected by said first detection circuit for output, and selecting difference data output from said subtracter at a timing other than the timing detected by said first detection circuit for output; a second retain circuit [104, fig. 1]storing previous data output to said processing unit; and an adder adding difference data output from said random access memory and said previous data stored in said second retain circuit [col. 2, lines 40-60; col. 3, lines 1-45].

6. As per claim 10-12:

Claims 10-12 are rejected for the same reasons as set forth for claims 1-3 due to the same scope.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 8 are rejected under 35 U.S.C 103(a) as being unpatentable over Al-Shamma, , in view of Takahashi et al PN 6,005,623, and further in view of Igarashi et al PGPUB 20020090142.

7. As per claims 5, 8:

Al-Shamma teaches the claimed limitations as noted above.

Al-Shamma does not teach a variable-length coder applying variable-length coding on difference data output from said subtracter for output to said random access memory, and a variable-length decoder applying variable-length decoding on

variable-length coded difference data output from said random access memory to output the decoded data to said adder.

Takahashi teaches variable length coder [85, fig. 1B] applying variable-length coding on difference data output from said subtracter [20, fig. 2C; col. 8, lines 20-30] for output to said random access memory [78, fig. 2A], and a variable-length decoder [11, fig. 2B] applying variable-length decoding on variable-length coded difference data output from said random access memory to output the decoded data to said adder [13', fig. 2B]; [col. 2, lines 26-50; col. 8, lines 10-20; col. 23, lines 21-45].

Igarashi teaches variable length code encoder to minimize power consumption [abstract; summary of invention].

It would have been obvious to one having ordinary skill in the art at the time the invention was to include the coder/decoder variable length taught by Takahashi and Igarashi into Al-Shamma's data processor in order to reduce number of cycles required for acquisition of the coding/decoding processing operation (without prolonging the total processing time), therefore minimize power consumption of the system [Igarashi, summary of invention].

Allowable Subject Matter

8. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. AL-Shamma et al PN 6,611,473 discloses Power saving mode for memories.

b. Miki PN 6,259,383 discloses logic circuit for reducing power consumption.

c. Norman PN 6,292,868 discloses system & method for encoding data to reduce power consumption.

d. Morinaka et al PN 6,055,422 discloses semiconductor and power reducing method.

e. Takashima PN 5,931,927 discloses reducing fluctuation of power by inverting bits in groups of data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (703) 305-3023. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

HIEP T. NGUYEN
PRIMARY EXAMINER
for

NGOC DINH
Patent Examiner
ART UNIT 2187
December 4, 2003

DONALD SPARKS
Supervisory Patent Examiner
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